[0015] FIG. **7** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a fourth embodiment of the invention;

[0016] FIG. **8** is a cross-sectional view schematically illustrating a power MOSFET according to a first variation of the fourth embodiment,

[0017] FIG. **9** is a cross-sectional view schematically illustrating a power MOSFET according to a second variation of the fourth embodiment;

[0018] FIG. **10** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a fifth embodiment of the invention;

[0019] FIG. **11** is a cross-sectional view schematically illustrating a power MOSFET according to a variation of the fifth embodiment;

[0020] FIG. **12** is a cross-sectional view schematically illustrating the configuration of a power MOSFET according to a sixth embodiment of the invention;

[0021] FIG. **13** is a plan view schematically illustrating the configuration of the power MOSFET according to the sixth embodiment;

[0022] FIG. **14** is a cross-sectional view schematically illustrating a power MOSFET according to a first variation of the sixth embodiment; and

[0023] FIG. **15** is a cross-sectional view schematically illustrating a power MOSFET according to a second variation of the sixth embodiment.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Embodiments of the invention will now be described with reference to the drawings. In the following embodiments, it is assumed that the first conductivity type and the second conductivity type are n-type and p-type, respectively. Like elements in the drawings are marked with like reference numerals.

First Embodiment

[0025] FIG. **1** is a cross-sectional view schematically illustrating a power MOSFET according to a first embodiment of the invention.

[0026] It is noted that FIG. **1** shows only the cell section of the power MOSFET. The same also applies to FIGS. **2** to **11** described below.

[0027] As shown in FIG. **1**, the power MOSFET **21** according to this embodiment includes an n-type semiconductor substrate **19**, which is illustratively an n-type silicon substrate. An n^+-drain layer **2** is formed as a first semiconductor layer in the lower surface of the lower portion of the semiconductor substrate **19**. A drain electrode **1** is provided as a first main electrode on the downside of the semiconductor substrate **19** so as to be in contact with the n^+-drain layer **2**.

[0028] Above the n^+-drain layer **2** in the semiconductor substrate **19**, a plurality of stripe-shaped p-pillar layers **4** (third semiconductor layers) are formed. The portion of the semiconductor substrate **19** between the p-pillar layers **4** constitutes a stripe-shaped n-pillar layer **3** (second semiconductor layer). Thus the n-pillar layers **3** and the p-pillar layers **4** are alternately and periodically arranged parallel to the upper surface of the semiconductor substrate **19** to form a superjunction structure. In the surface of both widthwise sides of each n-pillar layer **3**, a p-base layer **5** is formed as a fourth semiconductor layer like a stripe. In the surface of the p-base layer **5**, an n-source layer **6** is formed as a fifth semiconductor layer like a stripe. That is, the p-base layer **5** is selectively formed in part of the surface of the n-pillar layer **3**, and the n-source layer **6** is selectively formed in part of the surface of the p-base layer **5**.

[0029] A gate insulating film **8** illustratively made of silicon oxide film having a thickness of approximately 0.1 μm is formed on the semiconductor substrate **19**. On the gate insulating film **8** directly above the n-pillar layer **3**, a gate electrode **9** is formed as a control electrode. The gate electrode **9** is insulated from the semiconductor substrate **19** by the gate insulating film **8**. The gate electrode **9** extends like a stripe parallel to the n-pillar layer **3**, and extends from the edge of the directly overlying region of the n-source layer **6** formed in one side of the n-pillar layer **3** through the directly overlying region of the p-base layer **5**, the n-pillar layer **3**, and the p-base layer **5** to the edge of the directly overlying region of the n-source layer **6** formed in the other side of the n-pillar layer **3**. Thus the insulated gate structure composed of the p-base layer **5**, the n-source layer **6**, the n-pillar layer **3**, the gate insulating film **8**, and the gate electrode **9** constitutes a planar gate structure. The gate electrode **9** is surrounded by the insulating film, and a source electrode **10** is provided on this insulating film. That is, the source electrode **10** is provided on the upside of the semiconductor substrate **19**.

[0030] In the upper surface of the semiconductor substrate **19** directly above the p-pillar layer **4**, a trench **16** is formed. Part of the source electrode **10** is buried inside the trench **16**. That is, the source electrode **10** protrudes downward in the directly overlying region of the p-pillar layer **4**, and the protruding portion enters the trench **16**. The portion of the source electrode **10** located in the trench **16** constitutes a trench contact **17**.

[0031] A p^+-contact layer **7** is formed on the periphery of the bottom of the trench **16**, or the lower end of the trench contact **17**. The impurity concentration in the p^+-contact layer **7** is higher than the impurity concentration in the p-base layer **5**. The p^+-contact layer **7** is formed at a deeper position than the p-base layer **5**. That is, the p^+-contact layer **7** protrudes downward from the lower surface of the p-base layer **5**, and the lower surface of the p^+-contact layer **7** is located lower than the lower surface of the p-base layer **5**. The lower surface of the trench contact **17** is located lower than the lower surface of the n-source layer **6** and the upper surface of the p^+-contact layer **7**, and higher than the lower surface of the p-base layer **5** and the lower surface of the p^+-contact layer **7**. Thus the p-base layer **5**, the n-source layer **6**, and the p^+-contact layer **7** are connected to the trench contact **17**.

[0032] Next, the operation and effect of this embodiment are described.

[0033] In conventional structures, a trench is formed in the semiconductor substrate, a p^+-contact layer is formed at the bottom of the trench, and a trench contact connected to a source electrode is formed inside the trench, whereas the p^+-contact layer is located inside the p-base layer. Hence holes generated in the drift layer with a superjunction structure formed therein flow from the bottom of the p-base layer into the p-base layer, pass through the p-base layer and the p^+-contact layer, and then flow into the source electrode. However, this path has high resistance because the impurity concentration in the p-base layer is as low as approximately 1/100 of the impurity concentration in the p^+-contact layer. Hence the hole discharge resistance is also high. If the hole discharge resistance is high, holes are likely to be accumulated in the drift layer, and the positive charge of the holes